**Benchmark Applications for Synthesizeable VHDL Model**

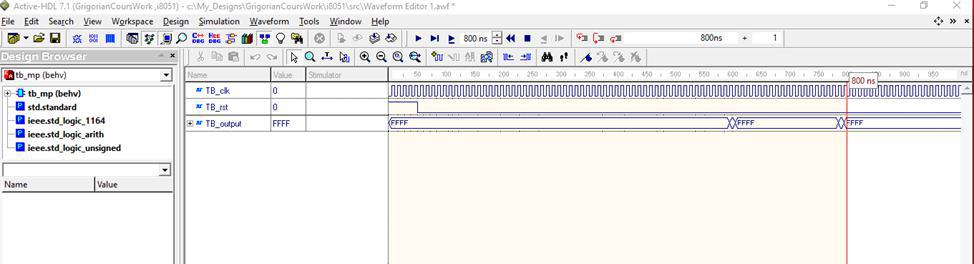
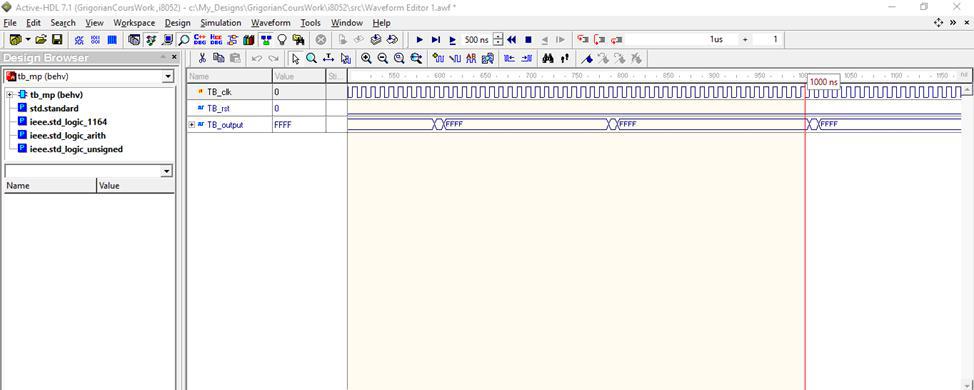
## Instructions for Using HEX Benchmarks

1. Convert benchmark hexfile into a VHDL ROM model
   * g++ -Wall i8052\_mkr.cc
   * a.out filename.hex
   * a file called i8052\_rom.vhd will be generated, copy this into your project directory
   * you will have to re-analyze the files (see above)
2. In the Synopsys VHDL Debugger
   * enter the time (in nanoseconds) that you want to simulate
   * Click on Run
   * The waveforms will appear in the Synopsys Waveform Viewer

## Instructions for Recompiling C code

1. Getting your C code ready to simulate (i.e. converting your C file to VHDL ROM model)
   * Compile your C file into Intel hex format (If you are using a KEIL compiler you can follow the steps below)
     + c51 filename.c
     + bl51 filename.obj to filename.abs
     + oh51 filename.abs
2. Follow instructions listed above for using hex benchmarks in order to convert hex file into VHDL ROM file.

## **Benchmarks Intel 8051**

**Benchmarks Intel 8052**